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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,946	04/13/2000	Maria Cristina B. Estacio	18865-004500US	6946
20350	7590 02/07/2002			
TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR			EXAMINER	
			PAREKH, NITIN	
SAN FRAN	CISCO, CA 94111-3834		ART UNIT	PAPER NUMBER
			2811	
		·	DATE MAILED: 02/07/2002	!

Please find below and/or attached an Office communication concerning this application or proceeding.



Office Action Summary

Application No. **09/548,946**

Applicant(s)

Estacio et al

Examiner

Nitin Parekh

Art Unit



•	- The MAILING DATE of this communication appears	on the cover sheet with the correspondence address
Period fo	• •	
THE MA	RTENED STATUTORY PERIOD FOR REPLY IS SET AILING DATE OF THIS COMMUNICATION.	
after: - If the pe	ons of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. Period for reply specified above is less than thirty (30) days, a reply insidered timely.	within the statutory minimum of thirty (30) days will
comn - Failure t - Any rep	nunication.	vill apply and will expire SIX (6) MONTHS from the mailing date of this cause the application to become ABANDONED (35 U.S.C. § 133). I date of this communication, even if timely filed, may reduce any
Status	a patent term adjustment. Geo or or vivo (b).	
1) 🗓 R	esponsive to communication(s) filed on <u>Nov 29, 20</u>	001
2a) 💢 T	his action is FINAL . 2b) ☐ This action	on is non-final.
	Since this application is in condition for allowance exclosed in accordance with the practice under Ex pai	cept for formal matters, prosecution as to the merits is rte Quay/1835 C.D. 11; 453 O.G. 213.
Disposit	ion of Claims	
4) 🗓 C	laim(s) <u>5 and 6</u>	is/are pending in the applica
4a) Of the above, claim(s)	is/are withdrawn from considera
5) □ C	laim(s)	is/are allowed.
6) 🗶 C	laim(s) <u>5 and 6</u>	is/are rejected.
7) □ C	laim(s)	is/are objected to.
8) 🗌 C	laims	are subject to restriction and/or election requirem
Applicati	ion Papers	
9) 🗌 T	he specification is objected to by the Examiner.	
10) 💢 T	he drawing(s) filed on Apr 13, 2000 is/ar	re objected to by the Examiner.
11) 🗌 T	he proposed drawing correction filed on	is: a∭ approved b)⊡disapproved.
12)□ T	he oath or declaration is objected to by the Examiner	r.
Priority ι	under 35 U.S.C. § 119	
13) 🗌 A	cknowledgement is made of a claim for foreign prior	ity under 35 U.S.C. § 119(a)-(d).
a)□	All b) Some* c) None of:	
1.	\square Certified copies of the priority documents have b	peen received.
2.	$\hfill\Box$ Certified copies of the priority documents have b	een received in Application No
	☐ Copies of the certified copies of the priority docu application from the International Bureau (the attached detailed Office action for a list of the co	(PCT Rule 17.2(a)).
	cknowledgement is made of a claim for domestic pri	
	-	,
Attachmer	•	40 T
		 18) Interview Summary (PTO-413) Paper No(s). 19) Notice of Informal Patent Application (PTO-152)
		20) Other:
		

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DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Temple et al (US Pat. 5103290).

Regarding claims 5 and 6, Temple et al disclose a chip device/package comprising:

- an integrated lead frame (96/98/94 in Fig. 12; Col. 8, line 39- Col. 9, line 45) having source (96 in Fig. 12) and gate (98 in Fig. 12) terminals/connections
- a bumped die (Fig. 2; Col. 4, line 5- Col. 7, line 5) including solder bumps (30/44 in Fig. 3-9; Col. 5, line 38- Col. 7, line 3; Col. 8, line 1-38) on top side, the die being attached/soldered to the base of the integrated lead frame such that the solder bumps contact respective source and gate terminals/connections
- a copper plate/frame (84 in Fig. 11 and 12; Col. 8, line 39- Col. 9, line 45) having a top surface soldered to the backside metallization of the die (Col. 8, line 57) and a bottom attached/bonded

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to the lead rail (82 in Fig. 11/12; Col. 8, line 44) using conventional processes such as soldering, brazing, etc. such that the copper plate contacts the drain region (metallization 14 at the backside of the die in Fig. 10-13)

(Fig. 1-13; Col. 4-14).

Temple et al disclose using a copper plate/frame connecting the backside of the die with the lead rail but fails to specify/designate the copper plate/frame as a copper clip.

The conventional components used in the chip interconnection/packaging art including conductive plate/strap, clip, frame/ring, etc. can be designated/specified according to the shape and function (reduced electrical resistance, stress relief, etc.) of the interconnecting components.

Therefore, it would have been obvious to a person of ordinary skill the art at the time invention was made to incorporate a copper clip attached/connected to the backside of the die to achieve the desired electrical resistance and bonding yield in Temple et al's device.

Response to Arguments

3. Applicant's arguments filed on 04-13-2000 have been fully considered but they are not persuasive.

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A. Applicant contends that it would not have been obvious to one of ordinary skill to use a copper clip in place of copper plate since copper plate of Temple et al provides the functions of providing an electrical connection to the drain and spreading the heat.

However, as explained above, it is conventional in the chip interconnection/packaging art to use components such as conductive plate/strap, clip, frame/ring, spring, etc. in a variety of different shapes and forms and such components provide electrical and mechanical functions including stress relief, component rework/removability, etc.

B. Applicant contends that Temple et al do not disclose a lead rail contacting the drain region of the die.

However, as seen from Fig. 12 in Temple et al's device, the copper plate/frame (84 in Fig. 11 and 12; Col. 8, line 39- Col. 9, line 45) having a top surface soldered to the backside metallization of the die (Col. 8, line 57) and a bottom being integrally attached/bonded to the lead rail (82/94 in Fig. 11/12; Col. 8, line 44) using conventional processes such as soldering, brazing, etc. such that the lead rail/copper plate contacts the drain region (metallization 14 at the backside of the die in Fig. 10-13). Furthermore, Temple et al disclose bending the rail portion of the lead frame/plate to provide a package with source, drain and gate terminals (Col. 9, line 20).

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Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

01-31-02

Tom Thomas Supervisory patent exampler Technology center 2800